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10/820,459	04/08/2004	Matthew Bellantoni	CDS-008	7251

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EXAMINER	
DAY, HERNG DER	
ART UNIT	PAPER NUMBER
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,459	BELLANTONI ET AL.	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/31/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-44 have been examined and rejected.

Information Disclosure Statement

2. The information disclosure statement filed January 31, 2005 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because the publication time cannot be identified for documents C2, C4, C19, C20, C43, C44, and C47. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Specification

3. The disclosure is objected to because of the following informalities. Appropriate correction is required.

3-1. It appears that "the destination variable(s) 248", as described at the last line of paragraph [0034], should be "the destination variable(s) 242".

3-2. It appears that "a hard device", as described at line 2 of paragraph [0041], should be "a hardware device".

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 28 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5-1. Claim 28 depends on itself. For the purpose of claim examination, the Examiner will presume that claim 28 is a dependent claim of claim 27.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-44 are rejected under 35 U.S.C. 102(e) as being anticipated by Neifert et al., U.S. Patent Application Publication No. 2004/0117168 A1, published June 17, 2004, and filed November 7, 2003.

7-1. Regarding claim 1, Neifert et al. disclose a method for optimizing a system-level simulation of a hardware device, the method comprising the steps of:

providing a system-level model ([0003]);

dividing the system-level model into a plurality of functional blocks ([0033]);

providing a mapping between the system-level model and each of the plurality of functional blocks ([0054]-[0059]);

compiling each functional block into at least one hardware object ([0064]-[0076]); and

linking the at least one hardware object with the system-level model ([0101]-[0108]).

7-2. Regarding claim 2, Neifert et al. further disclose wherein the at least one hardware object is expressed as compiled run-time code.

7-3. Regarding claim 3, Neifert et al. further disclose wherein each functional block is represented in at least one hardware description language.

7-4. Regarding claim 4, Neifert et al. further disclose wherein each functional block is represented in at least one high-level language.

7-5. Regarding claim 5, Neifert et al. further disclose wherein the high-level language comprises at least one of C, C++, SystemC, and Java ([0114]).

7-6. Regarding claim 6, Neifert et al. further disclose wherein the at least one hardware object comprises an API (Abstract).

7-7. Regarding claim 7, Neifert et al. further disclose wherein the APIs facilitate interface with application-level software programs ([0104]).

7-8. Regarding claim 8, Neifert et al. further disclose wherein each object API represents a pin-level interface corresponding to a hardware element ([0064]).

7-9. Regarding claim 9, Neifert et al. further disclose wherein the mapping step comprises at least one of the steps of API mapping and abstraction mapping ([0033]).

7-10. Regarding claim 10, Neifert et al. further disclose wherein the mapping step comprises API mapping, the API mapping step itself comprising:

receiving input data from the system-level model ([0033]);

translating the input data into a format readable by at least one hardware object ([0054]-[0055]);

providing the input data to the at least one hardware object ([0059]-[0064]); and

translating output data from the at least one hardware object into a format readable by the system-level model.

7-11. Regarding claim 11, Neifert et al. further disclose wherein (i) the system-level model comprises an API presenting an interface accurate with respect to boundaries of a system clock but having system-specific data and access requirements and (ii) the at least one hardware object comprises an API presenting an interface accurate with respect to boundaries of a system clock but having object-specific data and access requirements, the mapping step reconciling the requirements of the system-level API and each object-level API so as to facilitate data interchange therebetween while maintaining adherence to a system clock ([0027], [0033], [0039], [0059]).

7-12. Regarding claim 12, Neifert et al. further disclose wherein the mapping step comprises abstraction mapping, the abstraction mapping itself comprising an abstract interface to the system-level model and a pin-level interface to at least one hardware object ([0009]-[0013]).

7-13. Regarding claim 13, Neifert et al. further disclose wherein (i) the system-level model comprises an API presenting an interface accurate with respect to transactions and (ii) the at least one hardware object comprises an API presenting an interface accurate with respect to the boundaries of a system clock, the mapping step reconciling the transaction-based requirements of

the system-level API and the clock-based requirements of each object-level API so as to facilitate data interchange therebetween while maintaining adherence to the system clock ([0027]-[0032]).

7-14. Regarding claim 14, Neifert et al. further disclose comprising providing a control object, the control object controlling advancement of time and execution of transactions to thereby reconcile the transaction-accurate system-level API with the clock-based object-level APIs ([0050]-[0051]).

7-15. Regarding claim 15, Neifert et al. further disclose comprising the step of defining a mapping layer ([0054]).

7-16. Regarding claim 16, Neifert et al. further disclose wherein the mapping layer comprises a declaration module, a instantiation module, a sensitization module, an initialization module, an execution module, and an output scheduling module ([0054]).

7-17. Regarding claim 17, Neifert et al. further disclose wherein the declaration module defines a wrapper module inside the system-level model for accessing the at least one hardware object ([0075]-[0079]).

7-18. Regarding claim 18, Neifert et al. further disclose wherein the instantiation module creates an instance of the at least one hardware object, the at least one hardware object comprising at least one data structure, wherein the at least one data structure receives data from the mapping layer.

7-19. Regarding claim 19, Neifert et al. further disclose wherein the sensitization module detects a change to a pin of a pin-level interface to the at least one hardware object, the change

representing a signal which, if applied to a pin of a hardware element corresponding to the at least one hardware object, would affect an output pin of the hardware element.

7-20. Regarding claim 20, Neifert et al. further disclose wherein the change comprises assertion of at least one of (i) a clock signal, (ii) an asynchronous reset signal, and (iii) a signal affecting an output pin without requiring toggling of a system clock.

7-21. Regarding claim 21, Neifert et al. further disclose wherein the at least one hardware object comprises at least one data structure, wherein the initialization module assigns at least one value to the at least one data structure, thereby initializing the at least one data structure.

7-22. Regarding claim 22, Neifert et al. further disclose wherein the execution module copies input data from the mapping layer to the at least one hardware object, executes the at least one hardware object in accordance with the input data, and copies output data from the at least one hardware object to the mapping layer.

7-23. Regarding claim 23, Neifert et al. further disclose wherein the output scheduling module determines when output data is copied from the mapping layer to the system-level model.

7-24. Regarding claim 24, Neifert et al. disclose an apparatus for integrating a system-level simulation and a hardware device, comprising:

a system-level model divided into a plurality of functional blocks, each functional block being represented by at least one hardware object linked to the system-level model; and

a mapping layer between the system-level model and each of the plurality of functional blocks.

7-25. Regarding claim 25, Neifert et al. further disclose wherein each hardware object is expressed as compiled run-time code.

7-26. Regarding claim 26, Neifert et al. further disclose wherein each functional block is represented in a hardware description language.

7-27. Regarding claim 27, Neifert et al. further disclose wherein each functional block is represented in at least one high-level language.

7-28. Regarding claim 28, Neifert et al. further disclose wherein the high-level language comprises at least one of C, C++, SystemC, and Java.

7-29. Regarding claim 29, Neifert et al. further disclose wherein each hardware object comprises an API.

7-30. Regarding claim 30, Neifert et al. further disclose wherein the API facilitates interface with application-level software programs.

7-31. Regarding claim 31, Neifert et al. further disclose wherein the API is a pin-level interface corresponding to a hardware element.

7-32. Regarding claim 32, Neifert et al. further disclose wherein the mapping layer comprises an API mapping module configured to (i) receive input data from the system-level model, (ii) translate the input data into a format readable by a hardware object, (iii) provide the input data to the hardware object, and (iv) translate output data from the hardware object into a format readable by the system-level model.

7-33. Regarding claim 33, Neifert et al. further disclose wherein (i) the system-level model comprises an API presenting an interface accurate with respect to boundaries of a system clock but having system-specific data and access requirements and (ii) the hardware object comprises an API that presents an interface accurate with respect to boundaries of a system clock but having object-specific data and access requirements, the mapping layer reconciling the

requirements of the system-level API and each object-level API so as to facilitate data interchange therebetween while maintaining adherence to a system clock ([0072]-[0079]).

7-34. Regarding claim 34, Neifert et al. further disclose wherein the mapping layer comprises an abstraction mapping module that itself comprises an abstract interface to the system-level model and a pin-level interface to a hardware object ([101]).

7-35. Regarding claim 35, Neifert et al. further disclose wherein (i) the system-level model comprises an API presenting an interface accurate with respect to transactions and (ii) the hardware object comprises an API that presents an interface accurate with respect to the boundaries of a system clock, the mapping layer reconciling the transaction-based requirements of the system-level API and the clock-based requirements of each object-level API so as to facilitate data interchange therebetween while maintaining adherence to the system clock.

7-36. Regarding claim 36, Neifert et al. further disclose comprising a control object, the control object controlling advancement of time and execution of transactions to reconcile the transaction-accurate system-level API with the clock-based object-level APIs.

7-37. Regarding claim 37, Neifert et al. further disclose wherein the mapping layer comprises a declaration module, an instantiation module, a sensitization module, an initialization module, an execution module, and an output scheduling module.

7-38. Regarding claim 38, Neifert et al. further disclose wherein the declaration module is configured to define a template of the hardware object to facilitate interface with the system-level model.

7-39. Regarding claim 39, Neifert et al. further disclose wherein the instantiation module is configured to create an instance of the hardware object, the instance comprising a data structure configured to receive data from the mapping layer.

7-40. Regarding claim 40, Neifert et al. further disclose wherein the sensitization module comprises means enabling the mapping layer to detect a change to a pin of a pin-level interface of the hardware object, the change representing a signal which, if applied to a pin of a hardware element corresponding to the hardware object, would affect an output pin of the hardware element.

7-41. Regarding claim 41, Neifert et al. further disclose wherein the change comprises assertion of at least one of (i) a clock signal, (ii) an asynchronous reset signal, and (iii) a signal affecting an output pin without requiring toggling of a system clock.

7-42. Regarding claim 42, Neifert et al. further disclose wherein the hardware object comprises a data structure for receiving an initialization value from the initialization module.

7-43. Regarding claim 43, Neifert et al. further disclose wherein the execution module is configured to (i) copy input data from the mapping layer to the hardware object, (ii) execute the hardware object in accordance with the input data, and (iii) copy output data from the hardware object to the mapping layer.

7-44. Regarding claim 44, Neifert et al. further disclose wherein the output scheduling module is configured to determine when output data is copied from the mapping layer to the system-level model and to thereupon make the output data available to the system-level model.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

Reference to Parson, U.S. Patent 6,053,947 issued April 25, 2000, is cited as disclosing a method for simulating the operation of a circuit using a computer-based simulator.

Reference to Coppola et al., "OCCN: a NoC Modeling Framework for Design Exploration", Journal of Syatem Architecture, Volume 50, Issues 2-3, February 2004, pages 129-163, is cited as disclosing the on-chip communication network.

9. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kamini S. Shah can be reached on (571) 272-2279. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day
March 30, 2007

Thai Phan

THAI PHAN
PRIMARY EXAMINER
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